Test of a Low Current Amplifier ASIC for Cooled Large Area Potodiode

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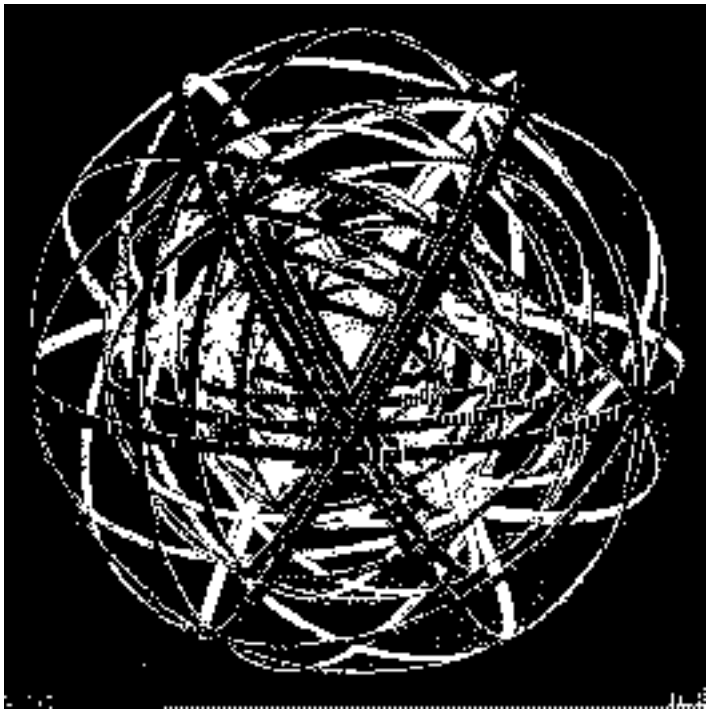

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Abstract

An ASIC has been designed, using the AMS 0.35 µ process, to provide an ultra low current amplifier for reading out a large area cooled photodiode. Our main goals were to have an input bias current at room temperature lower than 10 fA and a 0.1% signal-to-noise ratio for a few picoampere current measured during one second. We describe and interpret the tests which have checked that these figures were satisfied. These tests have allowed us to fix the few parameters which define an optimal filter. A stability problem remains at this prototype level, mainly related to the internal grounding scheme. It limit the range of photodiode capacitance usable when cascading the first stage and the second stage amplifiers belonging to the same chip. For the needs of the SNDICE project, which will be installed at the CFH telescope in fall 2007, a compact readout chain using the ASIC preamplifier has been developed and tested. It fulfills all the requirements of this project, in particular a 3 fA/$\sqrt{\text{hz}}$ and a 1.3 ms/$\sqrt{\text{pA}}$ sensitivity.

1 Introduction

The role of a Cooled Large Area Photodiode (CLAP) in the photometric calibration system proposed in [1], such as SNDICE[2], is both to provide a redundancy check of a focal plane calibration and to measure the optical transmission of the telescope independently of the detector and electronic efficiency (-cf. Appendix A). Its position inside the focal plane cryostat, or nearby, asks for the development of a compact electronic chain, as efficient as the best picoammeter in the market. We have proposed to integrate the two stages of a picoammeter - the low current preamplifier (LCA) and the amplifier on a CMOS asic. In fact we dispose of a large range amplifier based on a dual gain design[4]. In consequence we have developed an asic with an independent access to the two stages. We are studying here only the first stage for its new design, in order to qualify it completely.

2 Specifications

Our specifications include: a 10 fA sensitivity, a 18 bit dynamic range, a stability of baseline measurement and gain compatible with a 0.2 % accuracy on a year scale and a moderate power requirement. In any case a few external high precision passive components are needed, knowing the peculiarity of low current measurements (e.g. a 1GΩ resistor and a 4nF capacitor). However for a second step we are ready to integrate the output amplifier with the digitizer and the data transmitter functions, using the 12 bit ADC available to us on our AMS-O.35 µ analog asic process.

3 Test of Low Current Preamplifier

3.1 Input biases

The condition for being able to test the input bias current of the LCA ASIC is to have a test setup with a negligible leakage current. The ASIC being out of its support, the printed circuit board was tested by recording the currents flowing from the ground, or from the power supplies connector, to the LCA input signal connector submitted to a ±10V voltage, using Keithley 617 picoammeter. A <1pA transient current is recorded when voltage is applied, but it subsides in a few seconds and stabilizes around 20fA, which is the picoammeter pedestal value. (This could be the effect of loading the stray capacitance of the signal output through

the 1 GΩ feedback resistor).
Then the ASIC is put back in place and the same operation is repeated with a 1V voltage with the same result. At last the ASIC is powered and a 2.5 mV bias appears on the LCA input lead. Our conclusions are: test setup leakage resistance $>10^{14}\Omega$; voltage burden 2.5 mV; input bias current smaller or equal to a few femto-Amps. This last figure is well inside our target. It has to be confirmed in a real LCA configuration with a CLAP connected to the input by nulling the dark current and studying the pedestal stability of the photocurrent measurement.

3.2 Calibration of transimpedance and feed-back capacitance using current pulses

A square voltage pulse larger than 10 ms is applied to the signal input through a R_c=100 MΩ current calibration resistor. It creates a current pulse at the input of the ASIC, transformed to an output voltage pulse (see and Figure 1-a). The expected voltage gain is

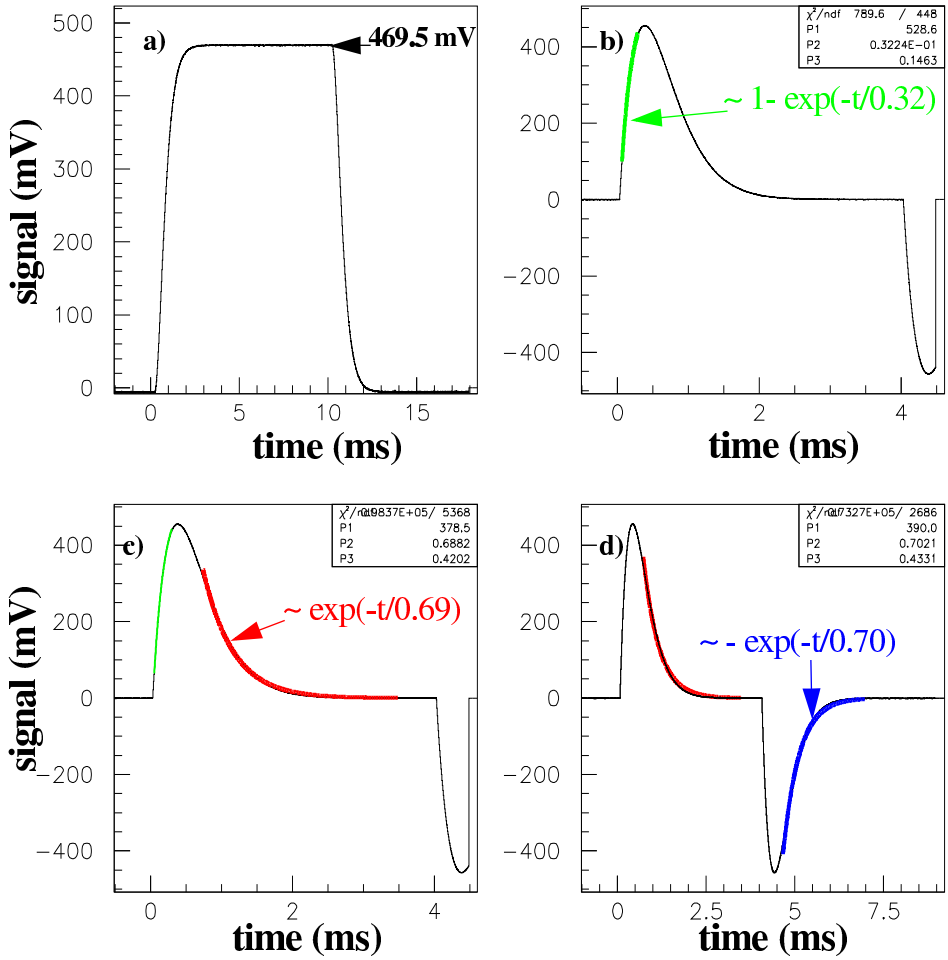

Figure 1 Calibration of current preamplifier (output filter 47 kΩx4.7 nF)
a) upper left: 10 ms current pulse 50mV/1MΩ, b) 4 ms charge pulse 50 mVx8.2 pF with rise-time fit, c)&d) idem with fits of decay-times

R_f/R_c= 10, where R_f= 1 GΩ is the feedback resistor. The measured gain is 9.4±2%, consistently with the precision of both resistors. The measured exponential rise/decay time is

R_fC_f= 0.7 ms telling us that C_f= 0.7 pF. The feed-back capacitance drawn inside the ASIC is 0.5 pF, the rest, i.e. 0.2 pF, is compatible with the expected (and small...) stray capacitance.

3.3 Calibration of input and feed-back capacitances using charge pulses

A 50 mV square voltage pulse is applied to the signal input through a C_c=8.2 pF charge calibration capacitor. It yields an output voltage peak of 820 mV, which decays exponentially (Figure 2). The measured exponential decay time is 0.69_3 ms (FWHM) telling us again that R_fC_f= 0.70 pF (see Figure 1-b,c,d and Figure 2). The voltage gain measured (820/50=16.4) is

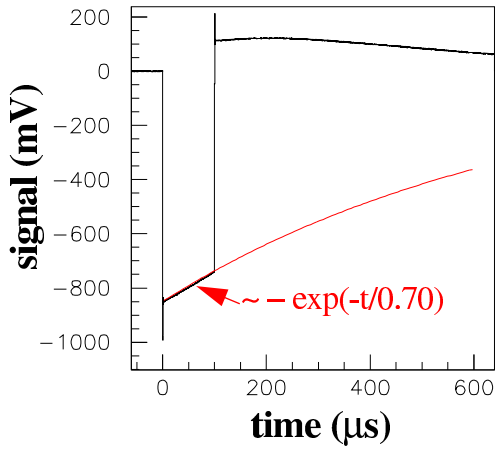

Figure 2 Calibration of current preamplifier (no output filter)
100 μs charge pulse 50 mVx8.2 pF with decay-time fit (rise-time 0.4 μs)

rather different than expected as the ratio C_d/C_f= 8.2/0.69=11.8.

3.4 Output noise

The noise measurement and the basic EMI control is done by digital signal processing as described in [4] and [5]. It covers a 3 hz to 400 Mhz range by joining frequency slices obtained in various runs with different sampling rates. This type of analysis works because of noise is decreasing with increasing frequency in such a way that aliasing noise does not swamp low frequency runs. In fact the low frequency analysis will be done in the next paragraph, on the complete system incorporating the low-pass filter needed for a low current preamplifier. This filter acts as an anti-aliasing filter for low frequency runs.
The system has three characteristic frequencies (in addition to the frequency of the low pass filter studied in § 3.4.3): a 20 Mhz DSA anti-aliasing filter, a 4 Mhz (RC=0.4ms) intrinsic band pass of the preamplifier in charge mode and a 2 khz (RC=0.7 ms) frequency of the current mode.

3.4.1 pickup noise

The high gain in the Mhz range, due to a small feedback capacitance, yield high sensitivity to ambient EMI noise. It is eliminated by filters inserted on both power supplies plugs. All classical precautions against low frequency noise -50 hz noise, microphonics, etc...- have to be taken, otherwise the preamplifier is just saturated! The EMI noise which remains is a mix of the 50 hz and of the 30 hz intrinsic to DSA scope. It dominates the noise figure of the pream-

plifier, even after the shields and the filters which have lowered that noise level by orders of magnitude (see Figure 3).

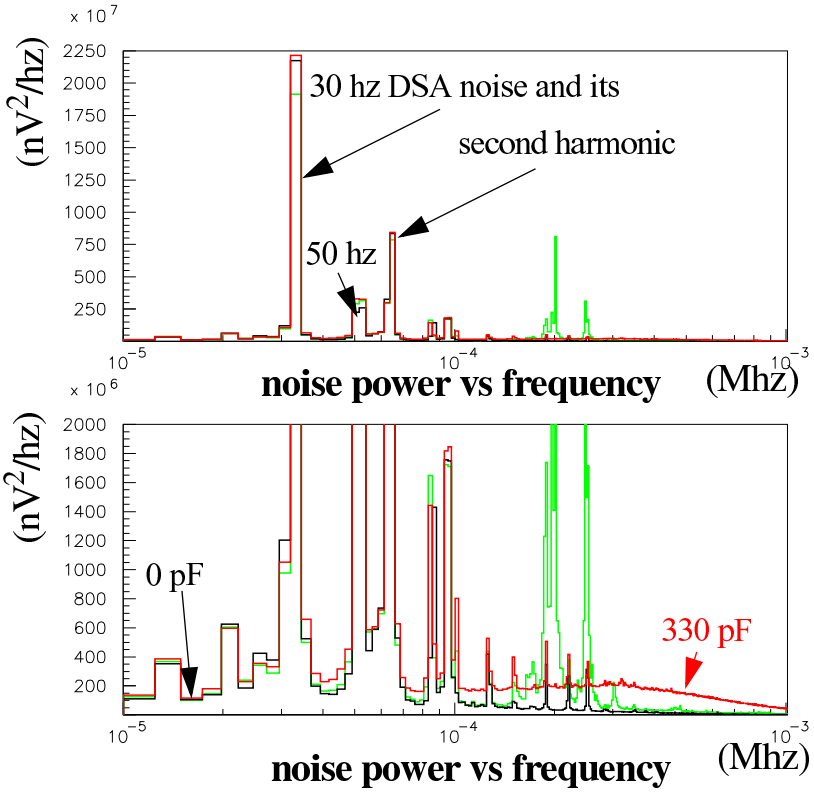

Figure 3 Pickup noise at low frequencies (with two different Y scales)

3.4.2 preamplifier noise

The remaining noise spectrum is plotted in Figure 4. The dominant high frequency and low frequency noise terms are respectively:

[1] $$en_1 = \frac{C_{in}+C_f}{C_f} \times \sqrt{8KT/3g_m} \qquad en_2 = \frac{1}{\omega \cdot T_f} \times \sqrt{4KTR_f}$$

where the series noise en_1 is due to the input FETs trans-impedance $1/g_m$ and the parallel noise en_2 to the R_f feedback resistor.

In fact the en_2 term can be understood as the asymptotic HF tail of the R_fC_f system $en_2' = \sqrt{4KTR_f/(1+(\omega \cdot T_f)^2)}$, which is the correct expression at all frequencies.

For each value of the input capacitance C_{in}, the average noise inside the 20-30 khz test window is computed and plotted as a function of C_{in} in Figure 5.

Considering the fall of the en_2' noise around $\nu = 2\pi R_fC_f$ and the constancy of the en_1, we have a noise corner at 3 khz, which is seen in Figure 6. In fact, from previous experience with AMS 0.35µ, the FET noise contains a 1/f contribution which generates generates a noise corner at exactly the same frequency. We have not made the studies allowing to separates FET 1/f from R_f noise.

The high frequency noise must be suppressed because otherwise it would saturate the second

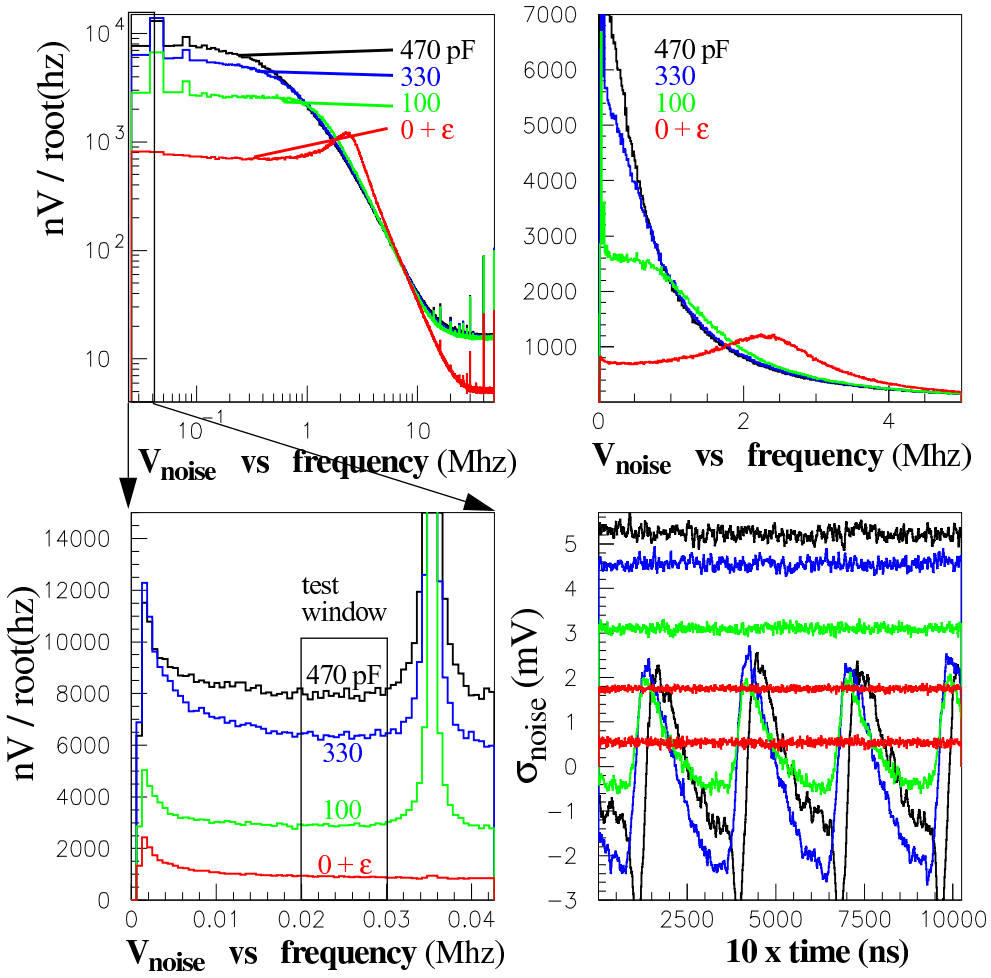

Figure 4 The preamplifier output noise spectrum is shown for various input capacitances at different frequency scales. High, medium and low frequency scales are shown respectively on top left, top right and bottom left. On bottom right the average and the root mean square of 2000 output signals digitized with a 8 bit/ 1 Ghz ADC, using the same color code as in the lower left plot. The extra (lower) red line corresponds to the same 0 pF input but filtered by the fast filter. The DSA digitizer is triggered on its own display sweep signal in order to identify and suppress the internal noise generated by this sweep.

stage of amplification. The optimization of the frequency cut-off depends of a detailed analysis of the experimental setup. It will be done at the end of the study.

3.4.3 noise after filtering

The effect of two simple RC filters -successively R= 11 kΩ & C=470 pF (RC=5.17 µs) and R= 47 kΩ & C=4.7 nF (RC=0.22 ms), is shown in Figure 6. One notice that, contrary to the fast filter, the slow one suppresses the noise corner. The noise reduction seen on the output RMS (Figure 4 lower right), goes from 1.8mV to 0.6 mV(RMS) with the fast filter but does not vary much passing from fast to slow filter because noise is globally dominated by pickup noise as mentioned in Section 3.4.1.

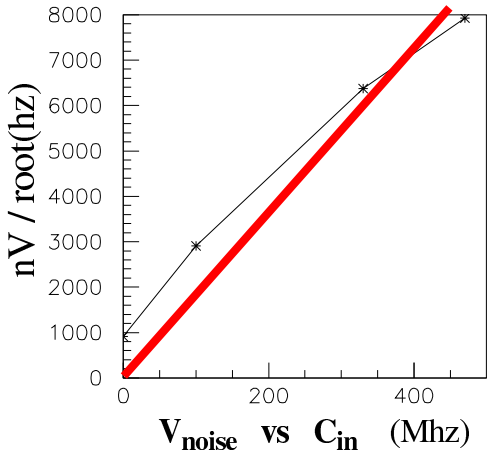

Figure 5 noise measured in test window (Figure 4) vs input capacitance C_{in} . In red equation the prediction of equation [1] .

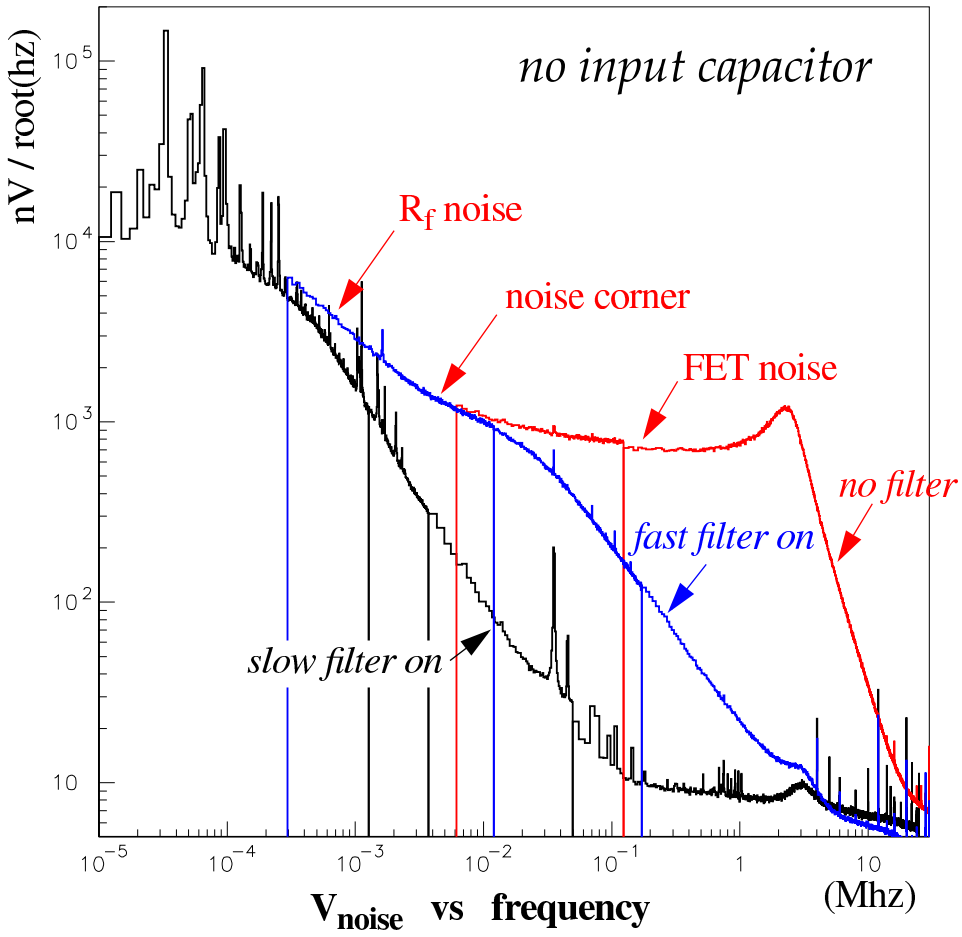

Figure 6 Noise spectrum with C_{in}=0: a) in red no filter, b) in blue fast filter (RC=4μs), c) in black slow filter (RC=0.2ms)

3.4.4 effect of input capacitance on filtered noise

The global behavior of a slow filter, almost matched to the R_fC_f cut-off of the square current pulses generated by LED illumination, is shown in Figure 7 for 0 pF, 100 pF and 330 pF (our

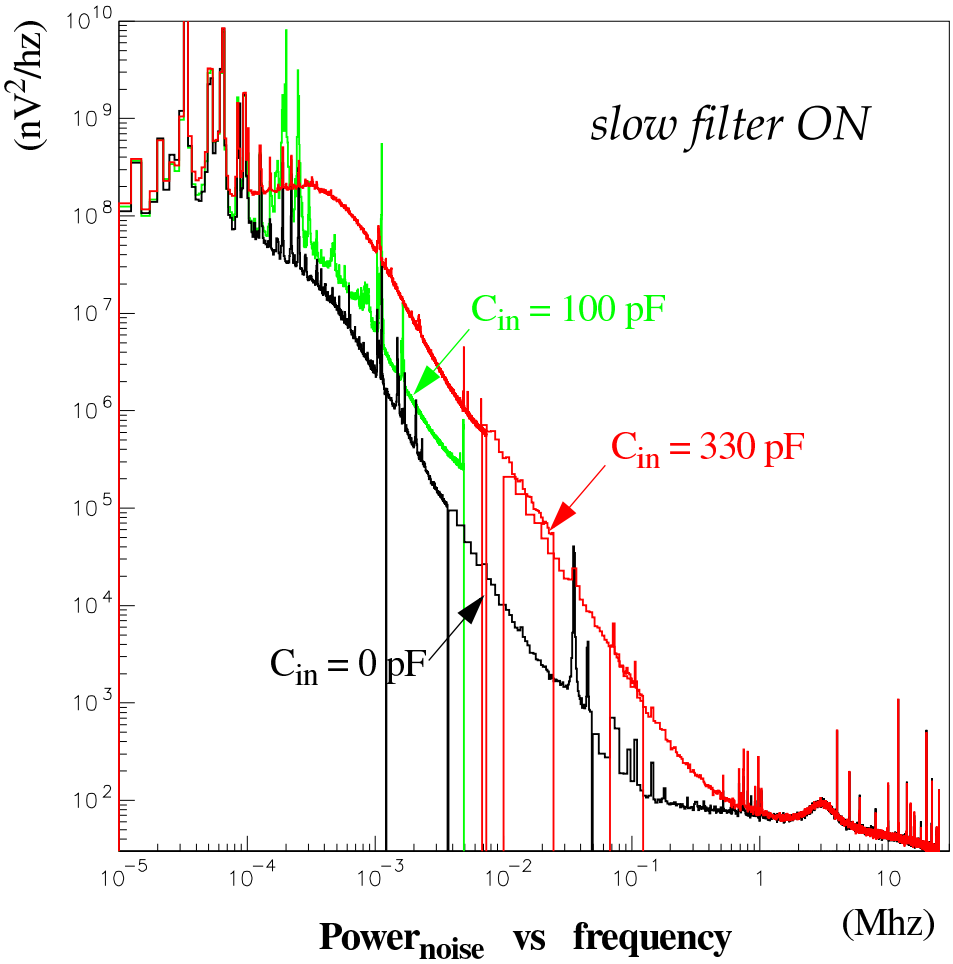

Figure 7 Preamplifier output noise spectrum a) in black input capacitance C_{in}=0, b) in red C_{in}= 330 pF, c) in green C_{in}= 100 pF

chosen CLAP photodiode). For 0 pF the dominating noise is Rf, for 330 pF it is FET and for 100 pF both contribute.

3.5 parametrisation of the preamplifier noise

The comparison between analytical formulas of § 3.4.2 and various spectra presented above are shown in Figure 8. We see a reasonable fit after modifying some of the electrical parameters. First in order to reproduce the low frequency behaviour we had to increase by a factor two the noise generated by the feedback resistor R_f (i.e. the noise of a 4GΩ instead of 1 GΩ). This is not shocking since a 1 GΩ resistor is certainly presenting extra noise compared to an ideal electron gas at 300K. High frequency noise is correct for the 100 pF configuration. however we had to create noise for the C_{in}=0 configuration using a fake value of parasitic capacitance of 25 pF, much bigger from what is known. This still insufficient to represent the 330 pF configuration (noise too small). At last we have a discrepancy around 3 khz corresponding to

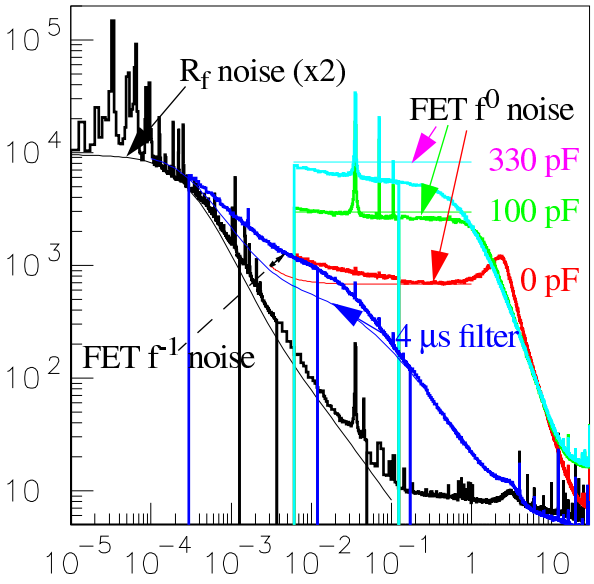

Figure 8 Two component model of preamplifier noise : analytic values are compared to measured spectra. The feedback resistor R_f noise is doubled. A 29 pF parasitic capacitance was added in order to represent artificially the "0 pF" noise. The transition region between these serial and parallel noise components is observed using the 4 µs filter. It shows the need for a third component ("1/f" like) around 100 khz.

missing noise. It is tempting to say that it is the contribution of 1/f noise. In fact it is exactly equal at 3 khz and above to what has been measured in a previous study of AMS 0.35m 1/f noise. However the discrepancy decreases below 3 khz, while 1/f noise is supposed to increase.
Finally our safer conclusion is that in the frequency range below 1 khz, which is our picoammeter range, our global noise resulting of feedback resistor and 1/f noise, is inferior or equal to twice the best theoretical value.

3.6 simulation of the preamplifier noise

On attend la simulation de Rachid Sefri.

4 Test of the Low Current Amplifier Chain

The LCA chain is made of the low current preamplifier studied above and the gain 3 amplifier situated in the same ASIC connected through a low pass filter (the "slow" filter of § 3.4.3).
A first series of tests with C_{in}=0 and a slow filter on gave results entirely consistent with those of Section 3.4.3, but for the gain. Then tests with C_{in}> 50 pF did show an oscillation which period is increasing with input capacitance. The instability itself is explained by the positive feedback between the output of the second stage voltage amplifier and the "ASIC ground" input of the first stage, by the voltage generated in the Asic-ground to ground parasitic resistance by the current flowing in the voltage feedback resistive chain. The corresponding waveforms are shown in Figure 9. The parasitic ground voltage is measured at the output of the three other amplifiers within the ASIC (which are not powered in this case). It reproduces the

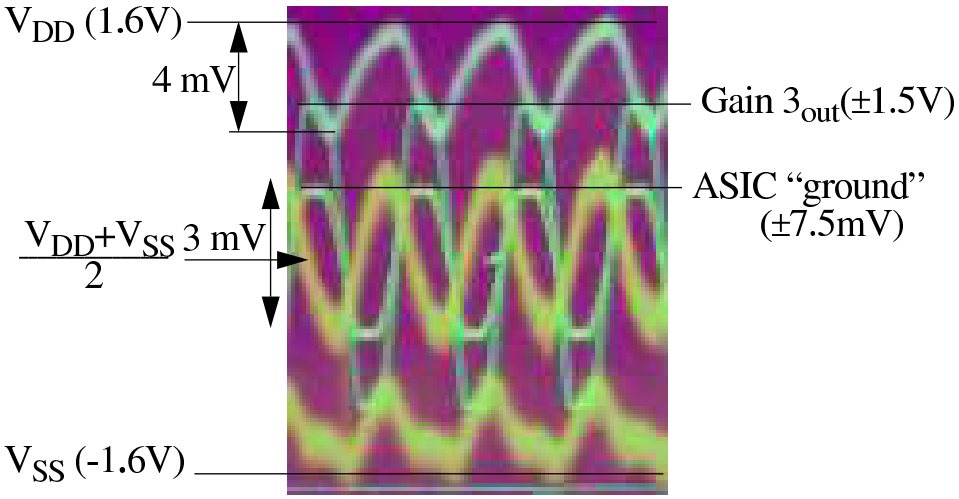

Figure 9 Oscillation of the system made by 1st and 2nd stage amplifier with 100 pF input capacitance

output with a 0.5% gain. This signs a parasitic resistance around 15 Ω . Coming back to C_{in}=0, we see in Figure 10 that, by sending a square input current pulse, the system has a tendency to oscillate. This effect can be reversed when the gain 96 amplifier is powered without being con-

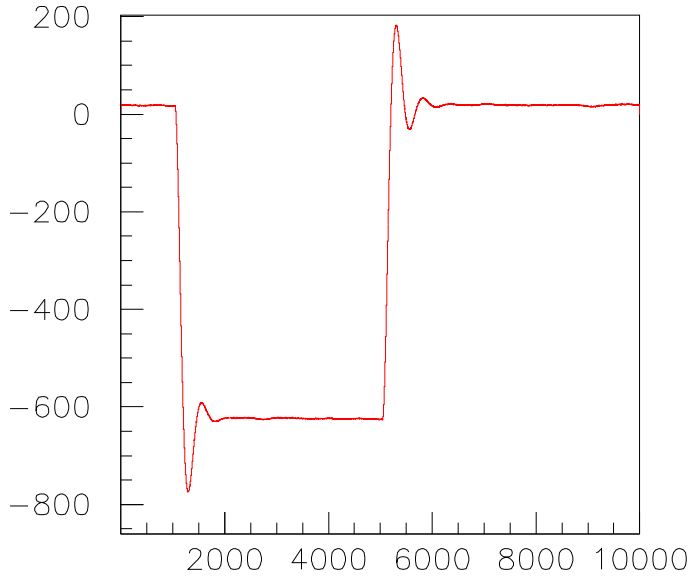

Figure 10 Output response of gain 3 amplifier to a square input current pulse

nected to the output of the preamplifier. Then it amplifies the parasitic feedback voltage but with a negative gain which turns out to be -1. Then just by coupling its output to ground, we can reverse the overall feedback voltage. This is one way, not the simplest, to achieve by an active mean an intrinsically stable integrated picoammeter design.

5 Test of CLAP prototype for SNDICE

The electronics for CLAP readout is composed of a front end card (see Figure 11), containing

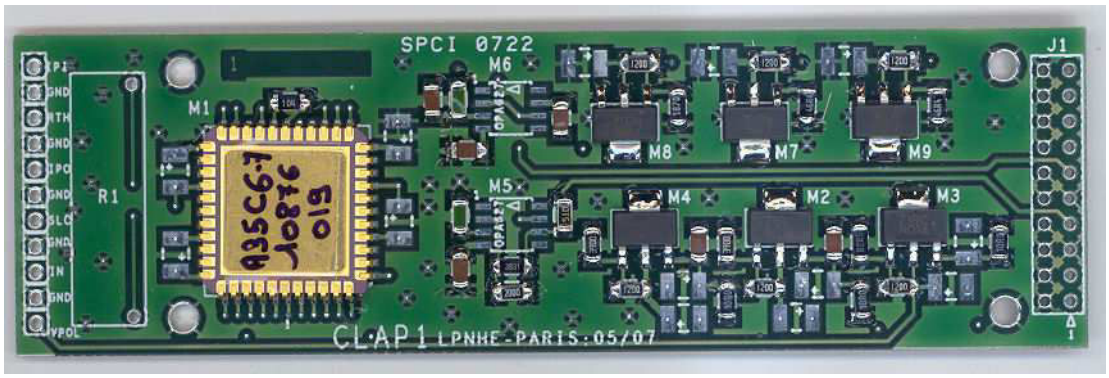

Figure 11 CLAP card (30x120 mm2) with the picoAmp ASIC on the left.

the ASIC preamplifier with its 1 GΩ feedback resistor, a gain 20 voltage amplifier and six local power supplies for the Asic and the photodiode.
The overall response of this amplification chain is stable. It has been tested under two configurations with a 1.78 ms and a 3.63 ms risetime, using respectively 1.5 and 3.3 pF feedback capacitors, as shown in Figure 12.

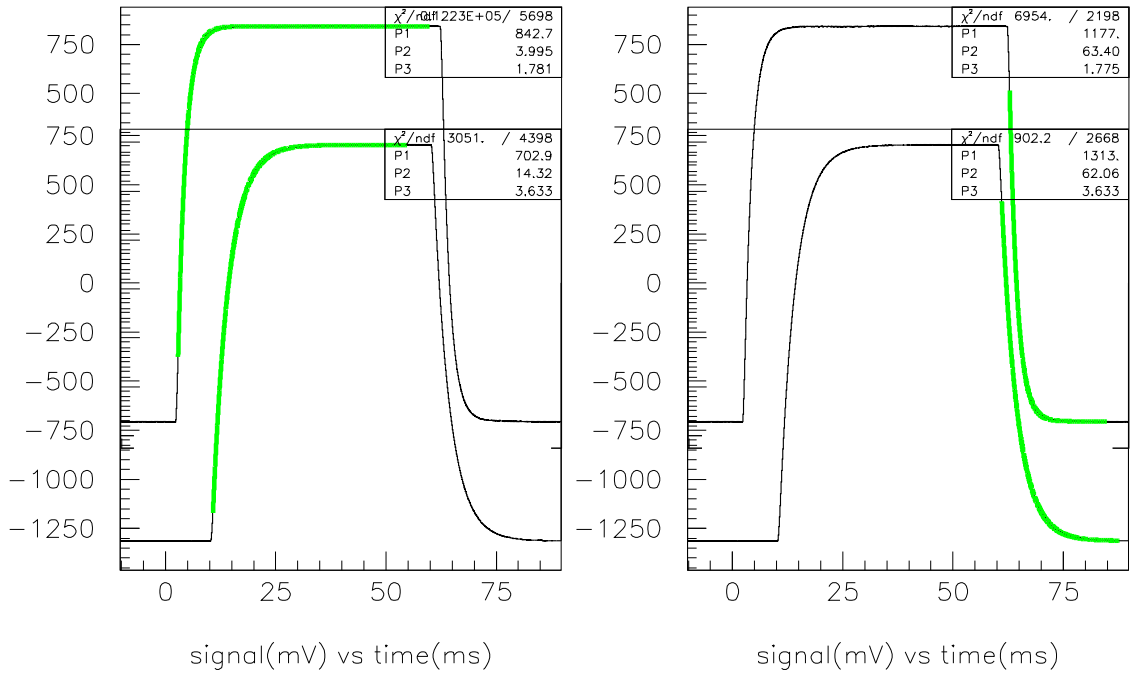

Figure 12 Amplifier output signal is 2 V for a 100 pA square input pulse (gain 20GΩ, 200 pulses averaged). Exponential fit of both edges give 3.633 ms rise&decay times with a 3.3 pF * 1 GΩ feedback and a 48 ms duration both in agreement with known characteristics. The underlying figure shows the output of a faster feedback chain (1.778 ms) obtained with a 1.3 feedback capacitor.

5.1 noise figure

Noise figures with fast and slow shaping are shown respectively in Figure 13 and Figure 14.

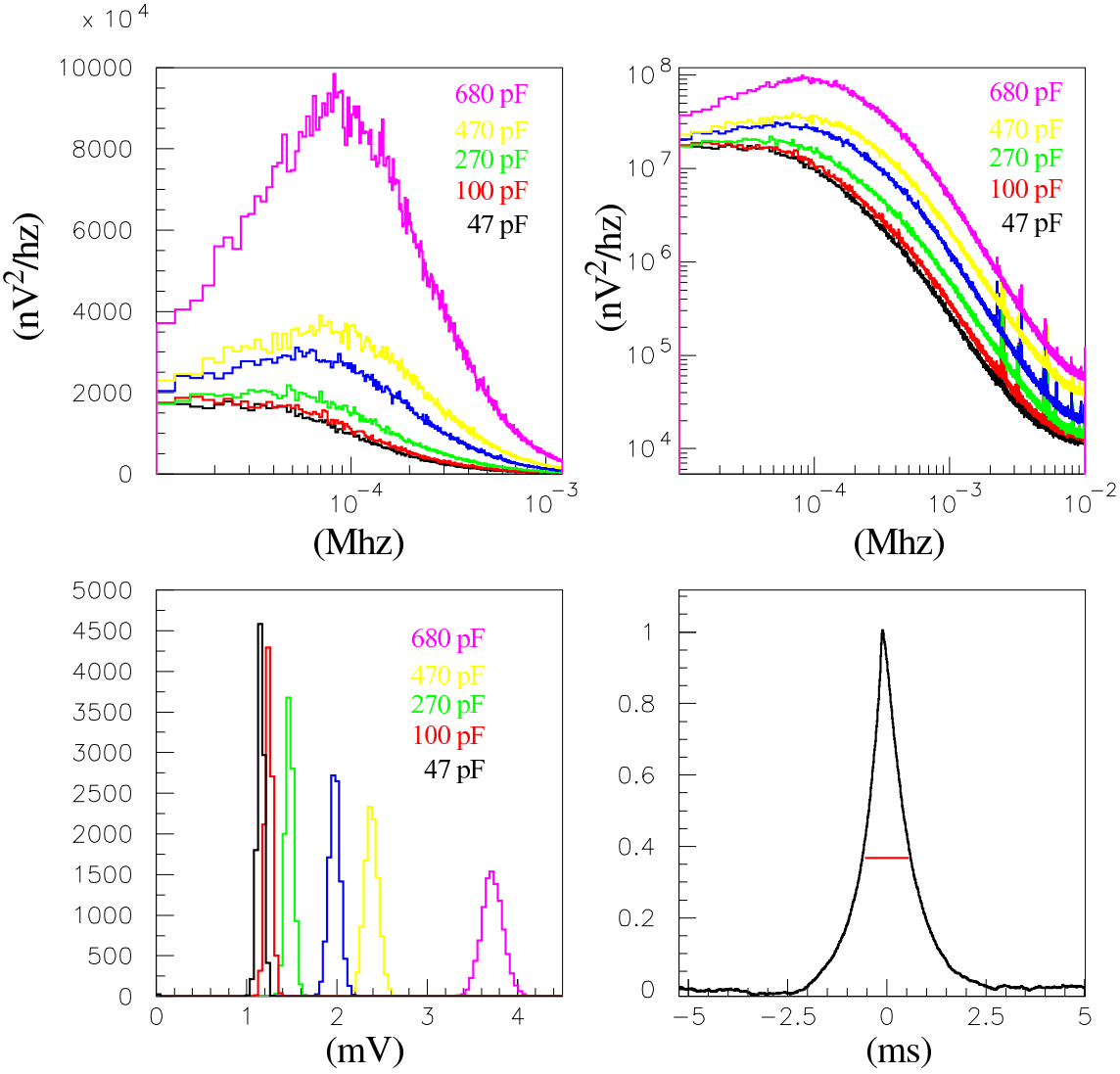

Figure 13 Top: preamplifier output noise spectra (C_{in} from 47pF to 680 pF; linear and log scales)
Bottom left: amplifier output noise (RMS voltage; C_{in} from 40pF to 680 pF)
Bottom right: autocorrelation fonction at C_{in}=680pF

Contrary to the analysis done with ASIC's gain 3 amplifier in § 3.5, these spectra are exactly compatible with algebraic formulas of § 3.4.2. There is no need for "extra noise" in the formulas. This is partly explained by the absence of microphonic noise, but probably also because of a good polarisation of the ASIC and the absence of internal parasitic feedback.
We want to optimize signal to noise ratio for square light pulses, considered either as a current measurement (flat top level related to absolute photodiode calibration) or as a charge measurement (integral of the pulse related to CCD pixel counts). Considering the expected 330 pF value of our photodiode capacitance, we prefered the slow shaping of Figure 14 which sacrifices a little the time resolution (cf. autocorrelation plot) for almost a factor two in output

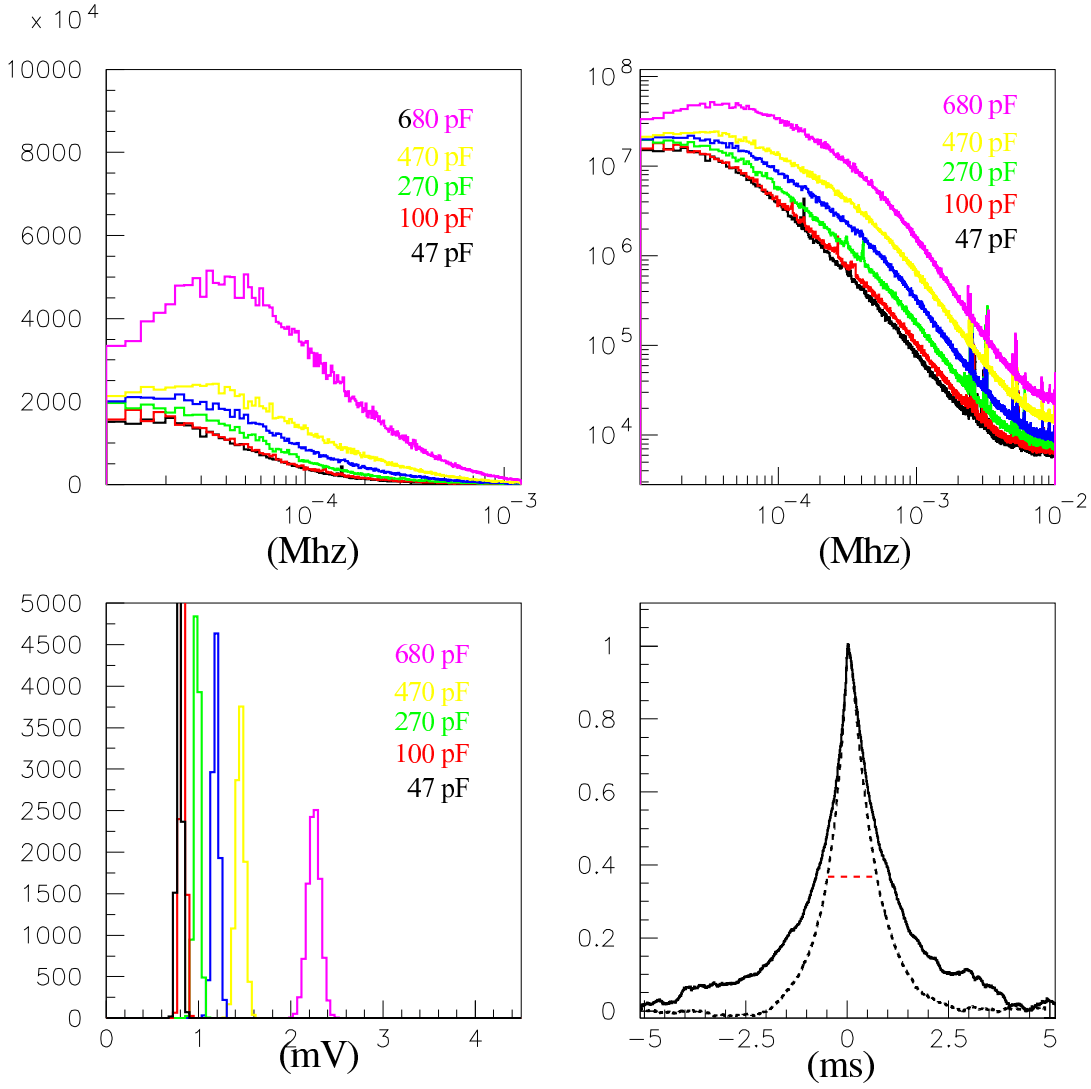

Figure 14 Same as Figure 13, but with a pramplifier feedback capacitor doubled

noise. These is explained by the effect of the feedback capacitor which filters more the series noise component than the parallel one.

5.2 noise induced by the polarization voltage

The photodiode is polarized by a DC voltage produced inside the CLAP card by a regulator. The output noise of the regulator, which is probably white, is introduced proportionally to the detector capacitance and amplified by our preamplifier with a gain equal to C_{in}/C_f (exactly like the input FET noise). This gain is enormous. Therefore the regulator noise dominates other types of noise studied so forth. We have confirmed this explanation by comparing regulator noise seen through two different capacitors (see Figure 15). Let us notice that this measurement separates the series noise component from the parallel one within of the noise model of § 3.5.

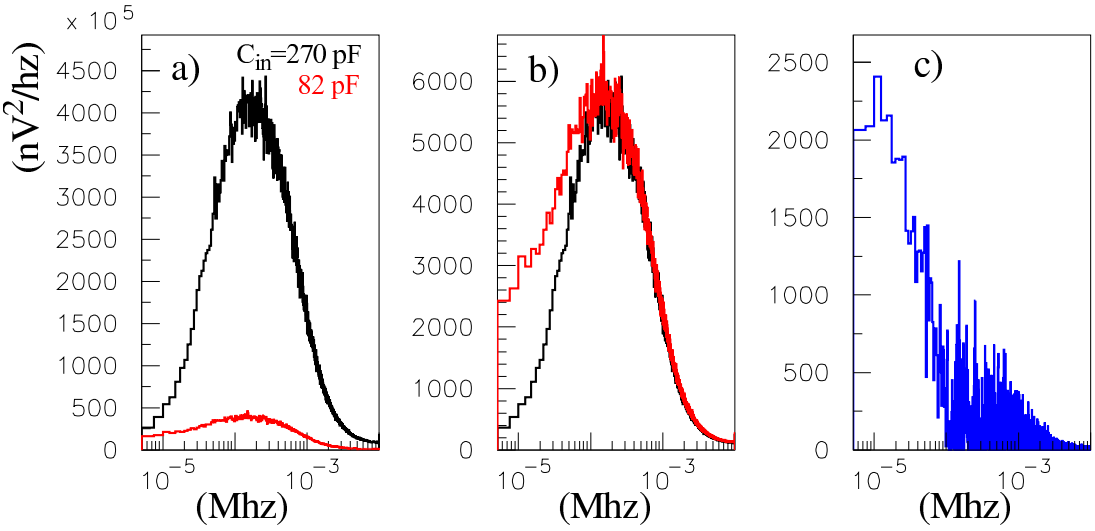

Figure 15 a) regulator noise injected through C_{in} capacitors (82 pF in red and 270 pF in black) b) same spectra rescaled by $(C_{in})^2$, c) R_f noise extracted by difference of rescaled spectra

5.3 low frequency noise and thermal sensitivity

The CLAP and its frontend electronics, including regulated power supplies, are conditioned in an aluminum box itself to be fixed on a metal structure. This assures a good thermal stability or at least a regular temperature variation on the scale of minutes. The main perturbations in the frequency range below one hertz are of thermal origin (vibration excluded). Therefore the current noise in the 0.1 to 10 hz is white and gaussian. It can be expressed by $\sigma \sim 3\,fA/\sqrt{hz}(RMS)$, for a 270 pF capacitor simulating the current source, as seen in Figure 16.

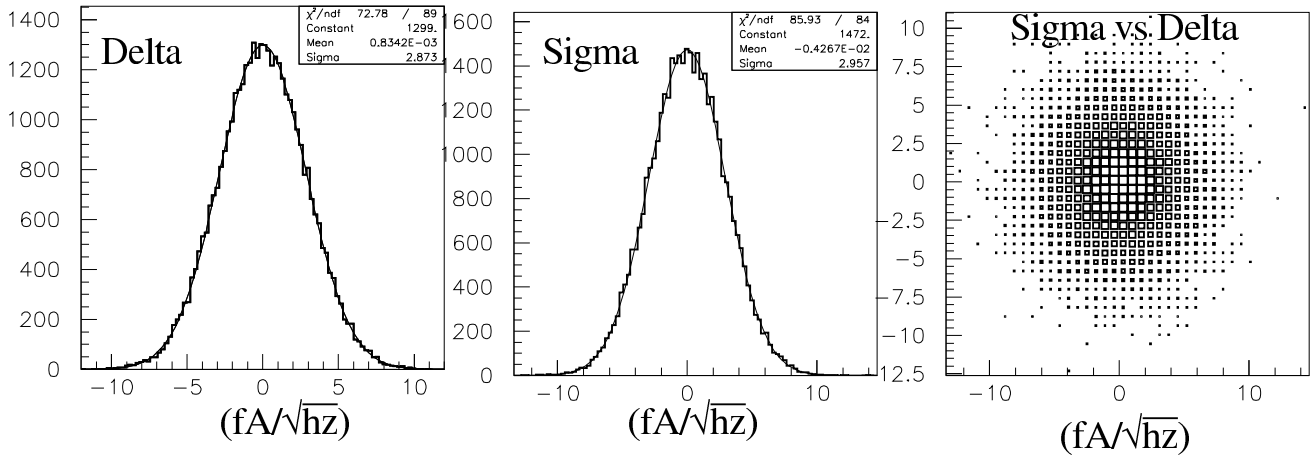

Figure 16 Low frequency noise analysis: the amplifier output is sampled numerically over 0.2 s intervals. Sigma and Delta are respectively the sum and difference of two adjacent samples expressed in fA/√hz at input are gaussian. Sigma is understood as a 0.4 s sample relative to a one minute average baseline. The Sigma vs Delta plot displays the "whiteness" of the noise (no autocorrelation at a 5 hz sampling frequency).

A long term recording of the baseline drift with the same setup shows (Figure 17) the effect of

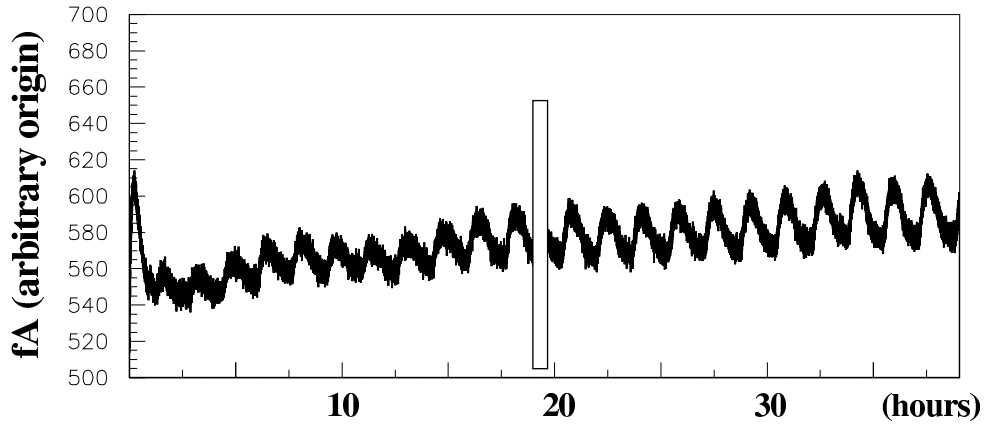

Figure 17 Baseline drift with a 270 pF capacitor simulating the current source

the 1 °C oscillation of CLAP temperature around 27 °C due to the air-conditioning of the lab's room. The parasitic dark current, flowing through the capacitor and the wiring, varies by ≈20 fA/°C. The part of this dark current originated in the ASIC is either much smaller or negligible. It would require a special experiment to measure it. With a photodiode cooled at minus 10 °C, in place of the 270 pF capacitor, the dark current jumps at 1.2 pA. Therefore the parasitic dark current is not presently a problem! It is foreseen that in the CFHT temperature environment all dark currents would be more than an order of magnitude smaller. However one should take some precautions against thermal fluctuations (large thermal capacitance connected to the CLAP, wind protection,...)

6 Conclusion

The two components of the ASIC under test, namely the current preamplifier and the dual gain voltage amplifier, work satisfactorily when separated but not when integrated.
The AMS 0.35m process has the FET electrical isolation performances which are required for the low current amplifier function.
In a first test configuration, using gain 3 amplifier inside the ASIC, we have measured an overall noise figure double of the analytical value (obtained when neglecting both the excess noise of the 1 GΩ resistor and the 1/f noise of the input FET). Later using an independant voltage amplifier (gain 20) on the ASIC board, we have measured the noise figure of an ideal 1GΩ resistor.
Therefore, in final analysis, the electronic noise generated inside the ASIC is perfectly understood. It does not appear in the overall noise budget for a detector capacitance below 500 pF. Waveform will be recorded at a few khz by a 16 bit ADC.
The single event sensitivity on the timing and amplitude measurements of a square light pulse are $\sigma_t \sim 1.3 ms/\sqrt{pA}(RMS)$ and $\sigma_I \sim 3 fA/\sqrt{hz}(RMS)$. It corresponds for our CCD calibration application to a 0.07 e^-/pixel/second flux.
Considering the repetitive nature of this measurement, the sensitivity can be brought further down by averaging multiple events.

With a few precautions, thermal drift effects should be negligible. In any case they wont be due to the ASIC.
Our digital signal processing analysis has produced a noise study across a nine decade frequency range. This method helped us with the optimization of the digitization chain for various detector capacitances, given the low current signal requirements (amplitude and rise time).
The tight schedule of the SNDICE project has imposed a temporary solution based on separating the preamp and the amplifier in order to solve the problem of common grounding inside the ASIC. However we can already propose a new ASIC design which will be free of this contingency. The dual gain amplifier contained in this ASIC, tested independently of the low current preamp, will then allow a 21 bit dynamical range instead of the 16 bit of the present device.

Appendix A: Cooled Large Area Photodiode (CLAP)

The necessity to cool a CLAP in order to suppress dark current is justified by the small photocurrent generated in the focal plane position. CLAPs can be mounted inside the camera's cryostat to share its cooling, or in a small vessel with a Thermo-Electric (T.E.) cooler and a temperature sensor (see Hamamatsu S3477 series). In the former case a Low Current Amplifier (LCA) adapted to the CLAP is the most convenient solution. This is the solution chosen for instance in the NIST amplifier for large area silicon photodiode described in [3]. It can be implemented with a commercial LCA with ultra low input bias current (few fA), in order to monitor photocurrent waveforms of transient LED illumination. The practical problem is that we have found only one such LCA (LCA-30-1T 10 fA) and it has a fixed gain which does not cover the whole CLAP signal range. In the latter case, an off-the-shelf picoammeter (Keithley Model 617 & 6514 3 fA) gives more versatility and performance. In our test bench we have developed a solution cumulating the advantages of both apparatus. It uses a dual gain amplifier [4] connecting the analog output of Keithley 617 Programmable Electrometer to two 16 bits digitizers. This provides a system adding a 0.5 Mhz/ 21 bits waveform digitizer to a Keithley preamplifier (low-input-bias-current/low-noise/programmable-gain/calibrated). On this line we are developing an ASIC integrating an ultra-low input bias current preamplifier with the dual gain amplifier and digitizer in order to equip several diodes on the same focal plane [2]. We expect a 1‰ electrical accuracy and a precision <1‰, with light-distance varying over a factor of 10 (current over a factor of 100). This corresponds to what is achieved with our current voltage measuring chain described in [5](chap.4). The irradiance versus distance relation offers a calibration of the pA range, in principle more accurate than Keithley's electrical calibration (2% accuracy).

Appendix B: Schematics for ASIC and test board

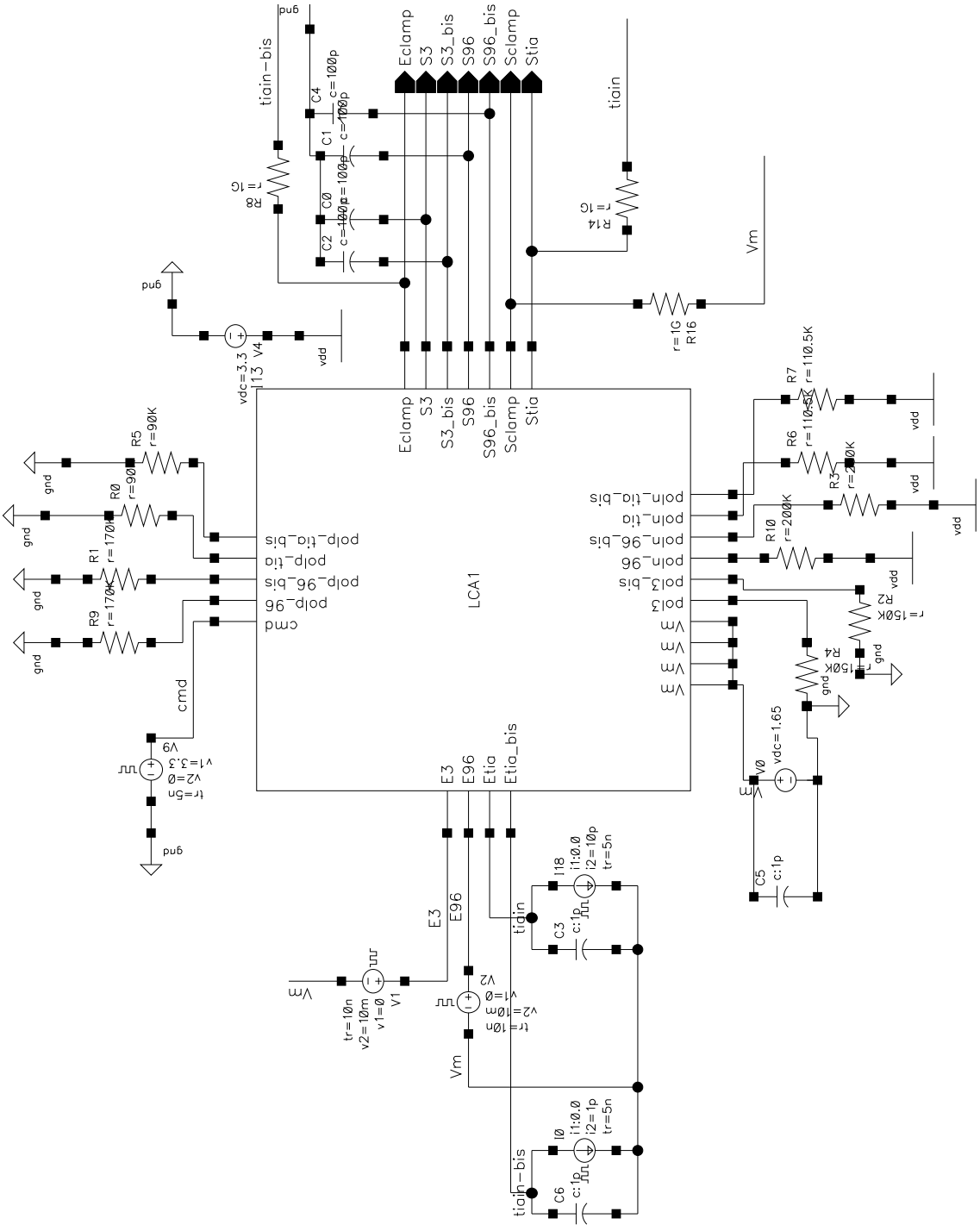

Figure 18 ASIC simulation layout

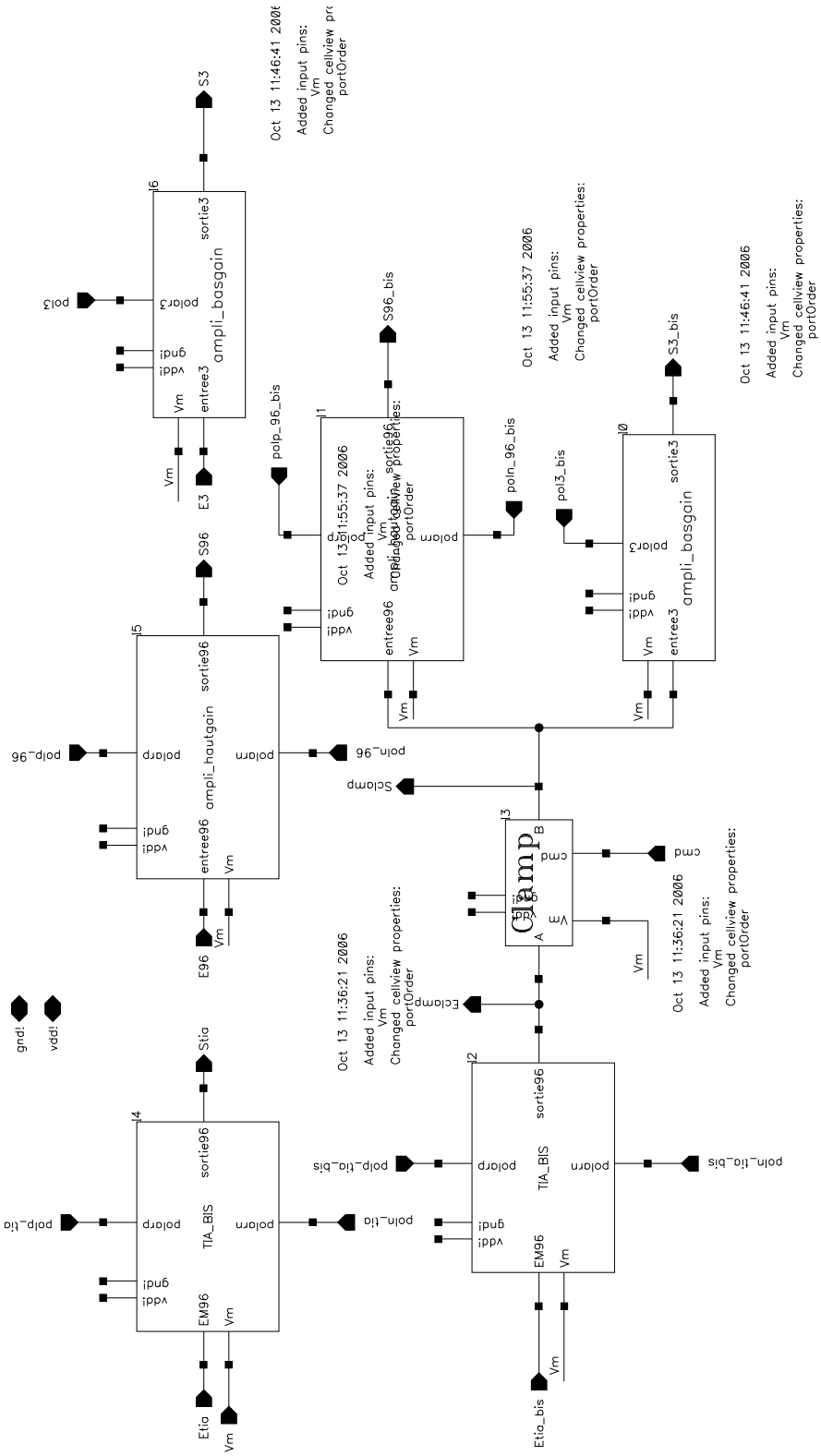

Figure 19 ASIC bloc diagram

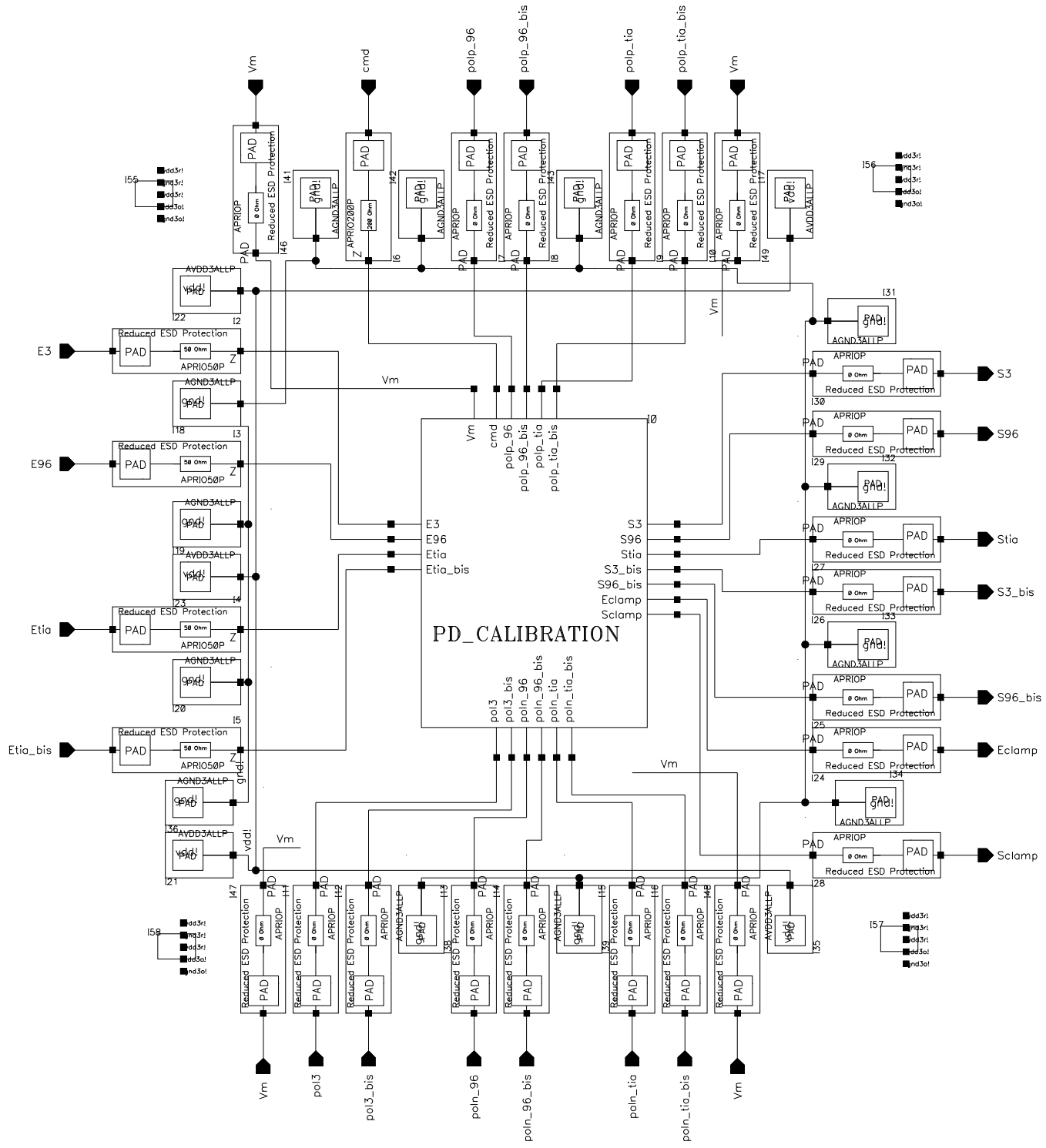

Figure 20 ASIC wiring

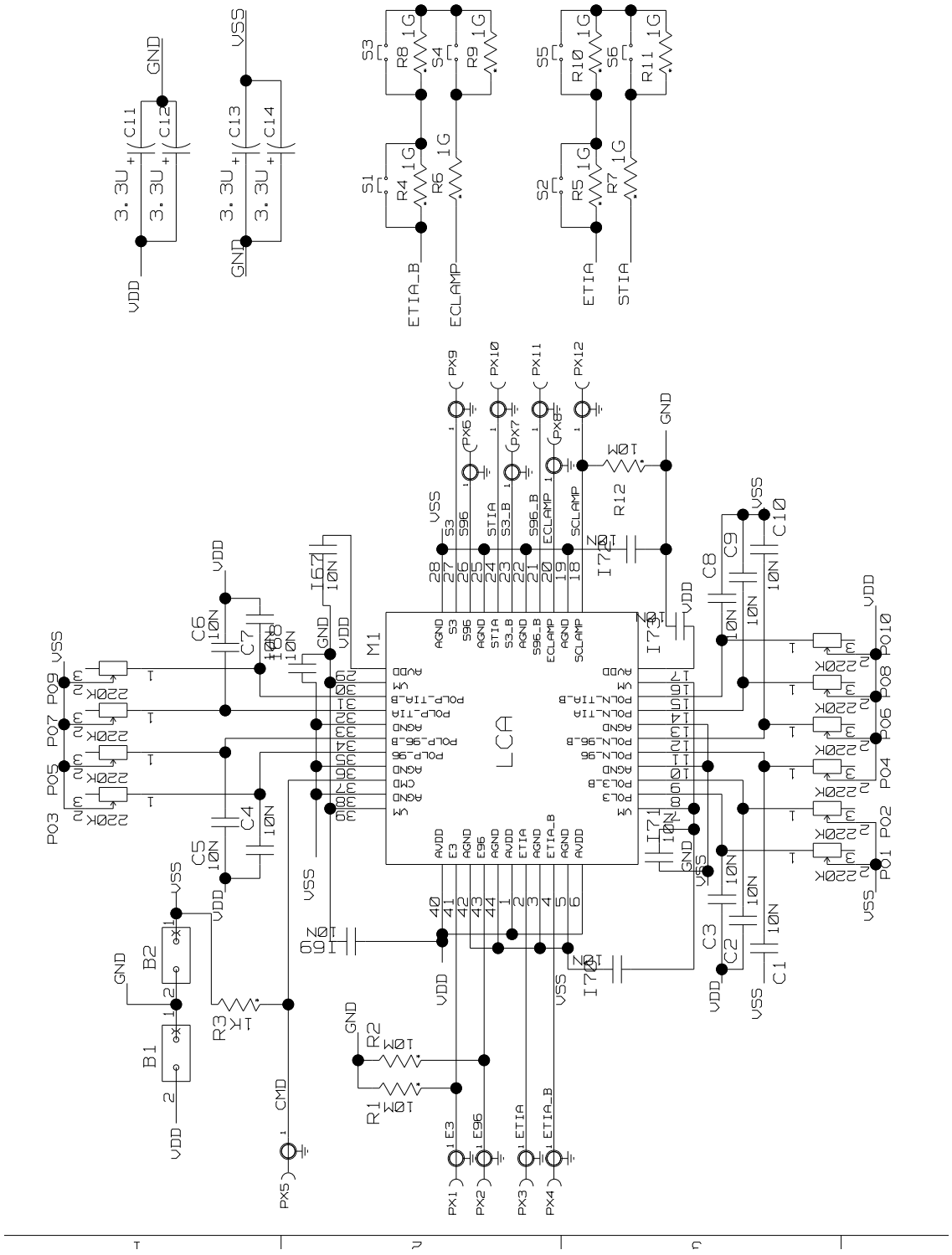

Figure 21 Test board schematic diagram

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